

Serial No. 10/733,381
Docket No. YOR920030503US1
YOR.494

2

AMENDMENTS TO THE CLAIMS:

1. (Currently amended) A method of forming a semiconductor structure, comprising:
providing a nitride layer between a silicon-containing layer and a polysilicon layer,
wherein said silicon-containing layer comprises a grain size substantially within a nano-
scale size.
2. (Original) The method of claim 1, further comprising:
forming an amorphous silicon layer, to provide said silicon-containing layer.
3. (Original) The method of claim 1, further comprising:
forming a polysilicon layer, to provide said silicon-containing layer.
4. (Original) The method of claim 1, further comprising:
forming a SiGe layer, to provide said silicon-containing layer.
5. (Original) The method of claim 1, wherein a grain size of said silicon-containing layer is
smaller than that of said polysilicon layer.
6. (Original) The method of claim 1, wherein said silicon-containing layer is formed below
said polysilicon layer.

Serial No. 10/733,381
Docket No. YOR920030503US1
YOR.494

3

7. (Original) The method of claim 1, wherein said nitride layer comprises a silicon nitride layer.

8. (Currently amended) The method of claim 1, wherein said semiconductor structure comprises a gate stack, and

wherein a grain size of said silicon-containing layer is smaller than that of said polysilicon layer.

9. (Original) The method of claim 1, wherein said nitride layer is formed on a surface of said silicon-containing layer and said polysilicon layer is formed on a surface of said nitride layer.

10. (Original) The method of claim 1, wherein said silicon-containing layer has a grain size substantially within a range of about 10 nm to about 20 nm.

11. (Original) The method of claim 5, wherein said grain size of said silicon-containing layer is substantially within a range of about 10 nm to about 20 nm.

12. (Original) The method of claim 1, further comprising:
depositing one of an amorphous Si, a polysilicon, and poly-SiGe as said silicon-containing layer.

Serial No. 10/733,381
Docket No. YOR920030503US1
YOR.494

4

13. (Original) The method of claim 12, wherein said one of the amorphous silicon, the polysilicon, and the poly-SiGe has a thickness of about 10 nm to about 20 nm.

14. (Original) The method of claim 1, wherein said nitride layer has a thickness within a range of about 5 Å to about 15 Å.

15. (Currently amended) The method of claim 1, further comprising:
forming said silicon-containing layer on a gate dielectric,
said gate dielectric being formed on a substrate,
wherein a grain size of said silicon-containing layer is smaller than that of said polysilicon layer.

16. (Original) The method of claim 15, wherein said substrate comprises any of a bulk silicon substrate, a silicon-on-insulator, and a SiGe substrate.

17. (Original) The method of claim 15, wherein said gate dielectric has a thickness within a range of about 9 Å to about 50 Å.

18. (Original) The method of claim 15, wherein said gate dielectric comprises any of an oxide, an oxynitride, and an oxide-nitride stack combination.

19. (Original) The method of claim 2, wherein said amorphous Si is deposited at a temperature below 550 °C.

Serial No. 10/733,381
Docket No. YOR920030503US1
YOR.494

5

20. (Original) The method of claim 3, wherein said polysilicon is deposited at a temperature below 550 °C.
21. (Original) The method of claim 12, wherein said nitride layer is formed by a furnace anneal on said one of the amorphous silicon, the polysilicon, and the poly-SiGe.
22. (Original) The method of claim 21, wherein said nitride layer is formed by said furnace anneal at a temperature within a range of about 550 °C to about 750 °C.
23. (Original) The method of claim 21, wherein said nitride layer is formed by said furnace anneal in an ammonia ambient.
24. (Original) The method of claim 22, wherein said nitride layer is formed by said furnace anneal for about 5 minutes to about 20 minutes.
25. (Original) The method of claim 24, wherein said nitride layer is formed by said furnace anneal for about 15 minutes.
26. (Original) The method of claim 1, wherein said polysilicon layer has a thickness within a range of about 80 nm to about 130 nm.
27. (Currently amended) A method of making a semiconductor structure, comprising:

Serial No. 10/733,381
Docket No. YOR920030503US1
YOR.494

6

forming a gate stack including a silicon-containing layer and a polysilicon layer with a nitride layer therebetween,

wherein a grain size of the silicon-containing layer is set without affecting a sets the polysilicon grain size of the polysilicon layer.

28. (Original) A method of forming a gate stack, comprising:

providing a nitride layer between a silicon-containing layer and a polysilicon layer,
wherein said silicon-containing layer has a grain size substantially within a range of about 10 nm to about 20 nm.

29. (Currently amended) A semiconductor structure, comprising:

a first polysilicon layer; a second polysilicon layer formed over said polysilicon layer;
and a nitride layer formed between said first and second polysilicon layers,
wherein a grain size of said first polysilicon layer is smaller than that of said second polysilicon layer, and

wherein said grain size of said first polysilicon layer comprises a grain size substantially within a nano-scale size.

30. (Original) The structure of claim 29, wherein said first polysilicon layer has a grain size substantially within a range of about 10 nm to about 20 nm.

31. (Original) The structure of claim 29, wherein said nitride layer has a thickness within a range of about 5 Å to about 15 Å.

Serial No. 10/733,381
Docket No. YOR920030503US1
YOR.494

7

32. (Original) The structure of claim 29, further comprising:
a gate dielectric on which said first polysilicon layer is formed; and a substrate on which
said gate dielectric is formed.
33. (Original) The structure of claim 32, wherein said substrate comprises any of a bulk
silicon substrate, a silicon-on-insulator, and a SiGe substrate.
34. (Original) The structure of claim 32, wherein said gate dielectric has a thickness within a
range of about 9 Å to about 50 Å.
35. (Original) The structure of claim 32, wherein said gate dielectric comprises any of an
oxide, an oxynitride, and an oxide-nitride stack combination.
36. (Original) The apparatus of claim 29, wherein said second polysilicon layer has a
thickness within a range of about 80 nm to about 130 nm.
37. (Original) A gate stack, comprising:
a first polysilicon layer; a second polysilicon layer; and a nitride layer formed between
said first and second polysilicon layers, wherein said first polysilicon layer has a grain size
substantially within a range of about 10 nm to about 20 nm.